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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,347	11/08/2003	Catherine B. Labelle	0180151	4624

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FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
CHEN, KIN CHAN	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,347	LABELLE ET AL.	
	Examiner	Art Unit	
	Kin-Chan Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *8-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *032105*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. Claims 8-14 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 1-7. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6, 7, 8, 13, and 14 are rejected under 35 U.S.C. 102(e) as anticipated by Colombo (US 2005/0079696).

In a method for forming a MOS FET on a substrate, Colombo teaches that a high-k dielectric layer may be situated over the substrate. A gate electrode layer (such as polysilicon) may be thereon. The gate electrode layer and high-k dielectric layer may be etched to form a gate stack. A nitridation process may be performed on the gate stack. Colombo teaches various high-k dielectric materials, reading on instant claims. See abstract; Fig.4; [0010] [0012] [0025] [0029].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-5, 9-12, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colombo (US 2005/0079696) in view of Alers et al. (US 6,265,260), Tu et al. (US 6,566,250) or Yeh (US 6,162,717).

In a method for forming a MOS FET on a substrate, Colombo teaches that a high-k dielectric layer may be situated over the substrate. A gate electrode layer (such as polysilicon) may be thereon. The gate electrode layer and high-k dielectric layer may be

etched to form a gate stack. A nitridation process may be performed on the gate stack. Colombo teaches various high-k dielectric materials, reading on instant claims. See abstract; Fig.4; [0010] [0012] [0025] [0029].

As to claims 2, 9, and 15, Colombo teaches nitridation may be accomplished by any suitable techniques [0011]. Hence, it would have been obvious to one with ordinary skilled in the art to use the conventional nitridation method of applying plasma comprising nitrogen. Alers et al. (US 6,265,260; col. 3, lines 41-43), Tu et al. (US 6,566,250; col.6, lines 7-9) or Yeh (US 6,162,717; col. 3, lines 40-49) is only relied on to show the conventional nitridation method of applying plasma comprising nitrogen. Because it is a conventional method in the art of semiconductor device fabrication and because it is disclosed by Alers, Tu, or Yeh, hence, it would have been obvious to one with ordinary skilled in the art to apply said nitridation method in the process of Colombo in order to efficiently carry out the nitridation process.

As to claims 3, 10, and 16, the prior art teaches the limitation because the same nitridation is performed on the gate stack, it is expected that the method of the prior art would contain the same properties and effects (nitrogen forming an oxygen diffusion barrier in the high-k dielectric segment).

Dependent claims 4, 5, 11, 12, 17, and 18 differ from prior art by specifying performing the nitridation and etching in the same process chamber or in the different chambers. However, it is merely a matter of choices of engineering depending on product specification and production requirement. In the absence of new or unexpected result, it would have been obvious to one with ordinary skilled in the art to perform

nitridation in-situ or ex-situ so as to meet the product specification and production requirement.

6. Claims 1, 7, 8, and 14 are rejected under 35 U.S.C. 102(b) as anticipated by Doyle et al. (US 5,891,798).

In a method for forming a MOS FET on a substrate, Doyle teaches that a high-k dielectric layer may be situated over the substrate. A gate electrode layer (such as polysilicon) may be thereon. The gate electrode layer and high-k dielectric layer may be etched to form a gate stack. A nitridation process may be performed on the gate stack. See abstract; col. 4 and col. 5.

7. Claims 2-6, 9-13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. (US 5,891,798) in view of Alers et al. (US 6,265,260), Tu et al. (US 6,566,250) or Yeh (US 6,162,717).

In a method for forming a MOS FET on a substrate, Doyle teaches that a high-k dielectric layer may be situated over the substrate. A gate electrode layer (such as polysilicon) may be thereon. The gate electrode layer and high-k dielectric layer may be etched to form a gate stack. A nitridation process may be performed on the gate stack. See abstract; col. 4 and col. 5.

As to claims 2, 9, and 15, Doyle teaches nitridation may be accomplished by any suitable techniques [0011]. Hence, it would have been obvious to one with ordinary skilled in the art to use the conventional nitridation method of applying plasma

comprising nitrogen. Alers et al. (US 6,265,260; col. 3, lines 41-43), Tu et al. (US 6,566,250; col.6, lines 7-9) or Yeh (US 6,162,717; col. 3, lines 40-49) is only relied on to show the conventional nitridation method of applying plasma comprising nitrogen. Because it is a conventional method in the art of semiconductor device fabrication and because it is disclosed by Alers, Tu, or Yeh, hence, it would have been obvious to one with ordinary skilled in the art to apply said nitridation method in the process of Doyle in order to efficiently carry out the nitridation process.

As to claims 6 and 13 and 19, Doyle (col. 4, line 2) teaches that any such high dielectric constant material can be used, making the claimed limitation obvious because the claimed high dielectric constant materials are commonly used in the art of semiconductor device fabrication.

As to claims 3, 10, and 16, the prior art teaches the limitation because the same nitridation is performed on the gate stack, it is expected that the method of the prior art would contain the same properties and effects (nitrogen forming an oxygen diffusion barrier in the high-k dielectric segment).

Dependent claims 4, 5, 11, 12, 17, and 18 differ from prior art by specifying performing the nitridation and etching in the same process chamber or in the different chambers. However, it is merely a matter of choices of engineering depending on product specification and production requirement. In the absence of new or unexpected result, it would have been obvious to one with ordinary skilled in the art to perform nitridation in-situ or ex-situ so as to meet the product specification and production requirement.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kin-Chan Chen whose telephone number is (571) 272-1461. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 4, 2005

K. C. Chen

Kin-Chan Chen
Primary Examiner
Art Unit 1765

K-C C